KS

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/520,677	03/07/2000	Garry Z. Gu	56115534-120430	9129

26291 7590 11/24/2003

MOSER, PATTERSON & SHERIDAN L.L.P.
595 SHREWSBURY AVE
FIRST FLOOR
SHREWSBURY, NJ 07702

EXAMINER	
VOLPER, THOMAS E	
ART UNIT	**PAPER NUMBER**
2665	12

DATE MAILED: 11/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

KS

Office Action Summary	Application No. 09/520,677	Applicant(s) GU, GARRY Z.	
	Examiner Thomas Volper	Art Unit 2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,10-12 and 15-17* is/are rejected.

7)☒ Claim(s) *6-9,13,14 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *11*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see REMARKS, 1st and 3rd paragraph under "Details of 103 Argument" heading, filed 18 August 2003, with respect to the rejection(s)of claim(s) 1 and 10 under U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made under Larsson et al. (US 6,172,963) in view of Caldara et al. (US 5,978,359). The Examiner acknowledges the deficiency of the Caldara reference in its failure to send the token bit in response to the second stage port processor receiving a data packet. However, the new grounds of rejection, Larsson et al. in view of Caldara et al., remedies this deficiency as evident from col. 5, lines 41-44 of Larsson. Specifically, Larsson discloses "the decision on how many cells should be sent during the next time interval also is based on how many cells actually have been granted transmission during the current time interval." In this example, the credits are established based on actual data cells, rather than a request packet. The combination of Caldara is now used simply to provide the ACCEPT/REJECT bit, which is considered to be the token bit of the present invention; and the Examiner holds that it would have been obvious to use this bit in determining credits. Although the Examiner has provided new grounds of rejection to meet the limitation of receiving a data packet, the Examiner respectfully disagrees with Applicant's argument that Larsson is "far too general" to suggest any of the limitations specifically claimed in the present invention. According to the MPEP, section 2111 [R-1], claims *must* be given their broadest reasonable interpretation. Larsson defines "giving credit" as determining a number of

cells that can be sent from each input port (col 3, lines 21-30). Larsson also discloses that the input ports may calculate how many cells can be permitted to be sent (col. 5, lines 12-23). This calculation of cells or credits represents the integrator block function of the present invention. The Applicant also argues that there is no specific organization of first stage and second stage port processors as in the present invention. Larsson discloses that calculating the number of cells to be sent to a particular output buffer includes determining which input ports should be allowed to send cells if several input ports are competing (col. 5, lines 31-36). The idea of several input ports competing for an output buffer matches the structure disclosed in claim 1 of the present invention of several neighboring integrator blocks figuring credits to send to a particular second stage port processor.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5, 10-12 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larsson et al. (US 6,172,963) in view of Caldara et al. (US 5,978,359).

Regarding claim 1, 10, 11 and 15, Larsson discloses a credit-based flow control system for a switch with input and output buffers. The input and output buffers represent the first and second stage port processors of the present invention. The system takes into account the degree of fullness of the output buffers when determining how many cells (credits) can be sent from

each input port. This process is called "giving credit" (col. 3, lines 21-30). With intelligence in the switch, it can be determined which output ports are able to receive cells (col. 4, lines 45-55). In the preferred embodiment, Larsson discloses a control unit (20) located in the switch core (8) for performing the intelligence. However, the intelligence may also be located outside the switch core and incorporated into the input buffers. In this case, the input ports would read the degree of fullness of the output buffers and calculate how many cells can be sent (col. 5, lines 12-23). This description meets the limitation of an integrator block in a first stage port processor, as in the present application. The limitation of neighboring integrator blocks is met by Larsson in that calculating the number of cells to be sent to a particular output buffer includes determining which input ports should be allowed to send cells if several input ports are competing for the output buffer (col. 5, lines 31-36). Larsson fails to expressly disclose sending a token bit from a second stage port processor to the neighboring first stage port processors. Caldara discloses a switching architecture that includes a first set of port processors, called To Switch Port Processors (TSPP) (14) and a second set of port processors, called From Switch Port Processors (FSPP) (16). These sets of TSPP's and FSPP's can be construed as representing first and second stages in the switch, respectively. Caldara also discloses a feedback message (30) that provides an indication of buffer status at the output port. To provide efficient flow control, the feedback message from the output port to the input port includes several sub-type messages, including an ACCEPT/ REJECT bit (col. 5, line 64 – col. 6, line 14). This bit is considered to provide the function of the token bit of the applicant's invention. Caldara discloses it is determined if the output buffers become filled to a threshold level when sending the feedback message in order to prevent cell loss (col. 4, lines 37-53). It is obvious that some component, such as a statistic block

as in the present application, must count the number of cells in the output buffers and compare them to a threshold level in order to obtain this result. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use the feedback message of Caldara in combination with the credit based flow control system of Larsson to provide a switch that selectively sends data from a first stage of input ports to a second stage of output ports in accordance with the fullness or availability of each output buffer. The feedback message of Caldara would notify the intelligent input ports of Larsson as to the availability of the output ports in order to calculate the credit given to each input port. One of ordinary skill in the art would have been motivated to do this to provide efficient flow control and avoid cell loss in the switch.

Regarding claims 2 and 3, Larsson discloses multiple input ports. The aforementioned teaching regarding claims 1, 10, 11 and 15 provides a description for the incorporation of intelligence into the input port. This description provides for an equivalent to neighboring integrator blocks.

Regarding claims 4, 5, 12, 16 and 17, Larsson discloses that the number of cells (credits) that can be sent are calculated for a time interval and depend on the number of cells already in the output buffers (col. 3, lines 45-58). It is possible, depending on the fullness of the output buffers from interval to interval, that the number of credits will change. This effectively achieves the process of incrementing and decrementing credits between time intervals.

Allowable Subject Matter

4. Claims 6-9, 13, 14 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 6, 13 and 14, the prior art fails to disclose sending a data packet from an input port to an output port having the maximum number of grant credits within the first stage.

Regarding claim 7, the prior art fails to disclose third stage port processors and that the statistics block accumulates real-time statistics of data packet departures to the third stage port processors.

Regarding claim 8, the prior art fails to disclose a relay from third stage port processors to first stage port processors, and sending the token bit from the third stage to the first stage.

Regarding claim 9, the prior art fails to disclose third stage switch elements on a single chip with first stage elements.

Regarding claim 18, the prior art fails to disclose that the statistics block departs the data packet that was sent that triggers a token bit to be sent.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Stephens et al. (US 6,345,040) Scalable Scheduled Cell Switch and Method for Switching

7. Any inquiry concerning this communication, or earlier communications from the examiner should be directed to Thomas Volper whose telephone number is 703-305-8405 and fax number is 703-746-9467. The examiner can normally be reached between 8:30am and 6:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu, can be reached at 703-308-6602. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4750.

Thomas E. Volper

TEV

November 13, 2003

HUY D. VU
PATENT EXAMINER
CENTER 2600